

**What is claimed is:**

1     A test circuit for a memory, which is incorporated  
into a semiconductor integrated circuit together with the  
5     memory, said test circuit comprising:

        a test signal generating circuit for generating a  
test signal for said memory, and a control circuit for  
conducting control of said test signal generating circuit;  
and

10          wherein a test setting mode and a test execution mode  
are switched to each other in accordance with a first  
control signal input from outside, and an initial data of  
the test signal and a control data for controlling said  
test signal generating circuit, which are input to said  
15     test signal generating circuit in said test setting mode,  
and a control data to said control circuit are input  
serially from an identical terminal.

2     A test circuit for a memory recited in claim 1,  
20     wherein said test signal generating circuit comprising a  
chip select signal generating circuit, an address signal  
generating circuit, a data signal generating circuit, and  
a read/write signal generating circuit.

25     3     A test circuit for a memory recited in claim 1,

characterized in that control of increment and decrement  
of an address, control of read/write and control of  
presence of a data reverse are performed in accordance  
with second, third and fourth control signals,  
5 respectively, which are input from outside.

4 A test circuit for a memory recited in claim 1,  
further comprising a selector for selecting an output data  
of a selected memory, and outputting it to outside as an  
10 output data.

5 A test circuit for a memory recited in claim 1,  
wherein said read/write signal generating circuit  
generates a read/write signal based on an output signal of  
15 said chip select signal generating circuit.